Application Note 80502

In-System Programming of PIC Microcontrollers

This application note describes how the PIC series of microcontrollers from Microchip Technology Inc. may be programmed in-circuit to production standards using the dedicated JTAG/ISP connector on the Pin-Master 48 universal programmer. The programming cable, the design of the target board, and programming procedures are described.
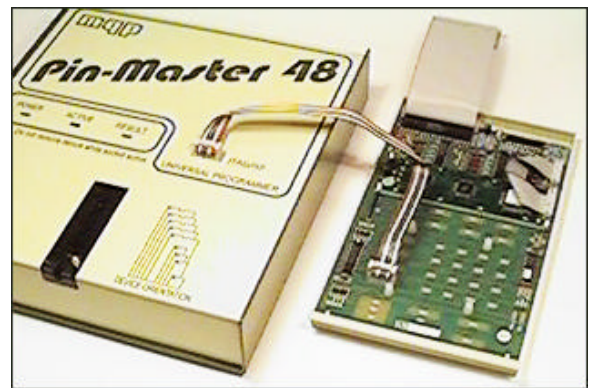
INTRODUCTION

The PIC series consists of a number of families of low cost, high performance, CMOS microcontrollers. They are available in a wide variety of packages with differing levels of peripherals integration. The majority of popular PIC family devices (see Table 1) can be serially programmed while in the end users target system.

In system programming reduces the number of times the parts have to be handled during the manufacturing process and allows the latest or custom software to be loaded just prior to shipping.

As a result of the short programming time, the use of a single site programmer with a dedicated ISP connector on a production line becomes an attractive and low-cost alternative to a separate gang programming operation.

However it is important to use a programmer capable of meeting the Microchip specification for production standard programming, such as the Pin-Master 48. Many other in-circuit programming solutions are only suitable for development programming, as they do not perform verification over a range of VDD voltages.

The serial interface between the programmer and target board is made up of two lines for clock and data, and three lines for power, ground and the programming voltage .

Production Programming using Pin-Master 48

The Pin-Master 48 universal programmer has a dedicated JTAG/ISP connector fitted to the top of the unit. A cable made up to the users own requirements connects the socket to the target board.

The requirements of in-system programming affects the circuit design of the target board. Aspects of the design which must be considered are explained in detail later in this application note.
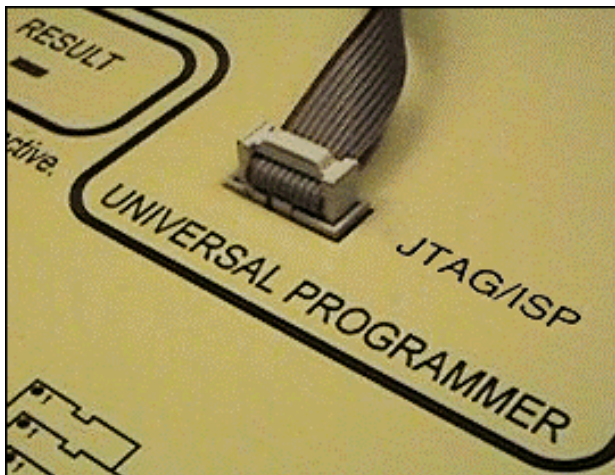
JTAG/ISP SOCKET

The socket is a standard 10 way 0.1″ header. A diagram of the socket is shown below:

Viewed from top, front of programmer

2 MODE	4 GND	6 GND	8 GND	10 GND
1 DET	3 VDD	5 DATA	7 CLK	9 VPP

1	DET	Cable Detect
2	MODE	Programming Mode
3	VDD	PIC Voltage Supply
4	GND	Ground
5	DATA	Data I/O
6	GND	Ground
7	CLK	Clock input
8	GND	Ground
9	VPP	Programming voltage
10	GND	Ground

CABLE

A ribbon cable with alternate wires connected to ground is used between the Pin-Master 48 and the target board. The cable should be kept as short as possible (maximum length 1.5m).

TARGET BOARD

Figure 3 shows a typical in-circuit serial programming connection. Its features are described in the following sections.

CONNECTOR

The target board should be equipped with a suitable connector. This could be most simply achieved with a similar connector and pin layout to that used at the programmer end of the cable.

- **GND Pins 4, 6, 8 and 10**

Connect these four pins to the target system ground.

- **MODE and DET pins**

The MODE and DET pins must be connected together on the target board. The presence of the link is detected by the programmer to confirm that the cable has been plugged into the target board.

The MODE pin is connected to ground at the programmer end of the cable. This signal may be utilised by the target board to switch the circuit into programming mode.

- **CLK**

Pin 7 of the ISP connector must be connected to the CLOCK pin (RB6) of the PIC. Any other circuit connected to RB6 for normal operation must have a minimum impedance of 10K when in the programming mode. This ensures that the logic level margins are maintained. It may be acheived by a series resistor, or by the intrinsic high impedance of the connected circuit (e.g. a logic input).

- **DATA**

Pin 5 of the ISP connector must be connected to the DATA pin (RB7) of the PIC. Any other circuit connected to RB7 for normal operation must have a minimum impedance of 10K when in the programming mode (see comments under CLK above).
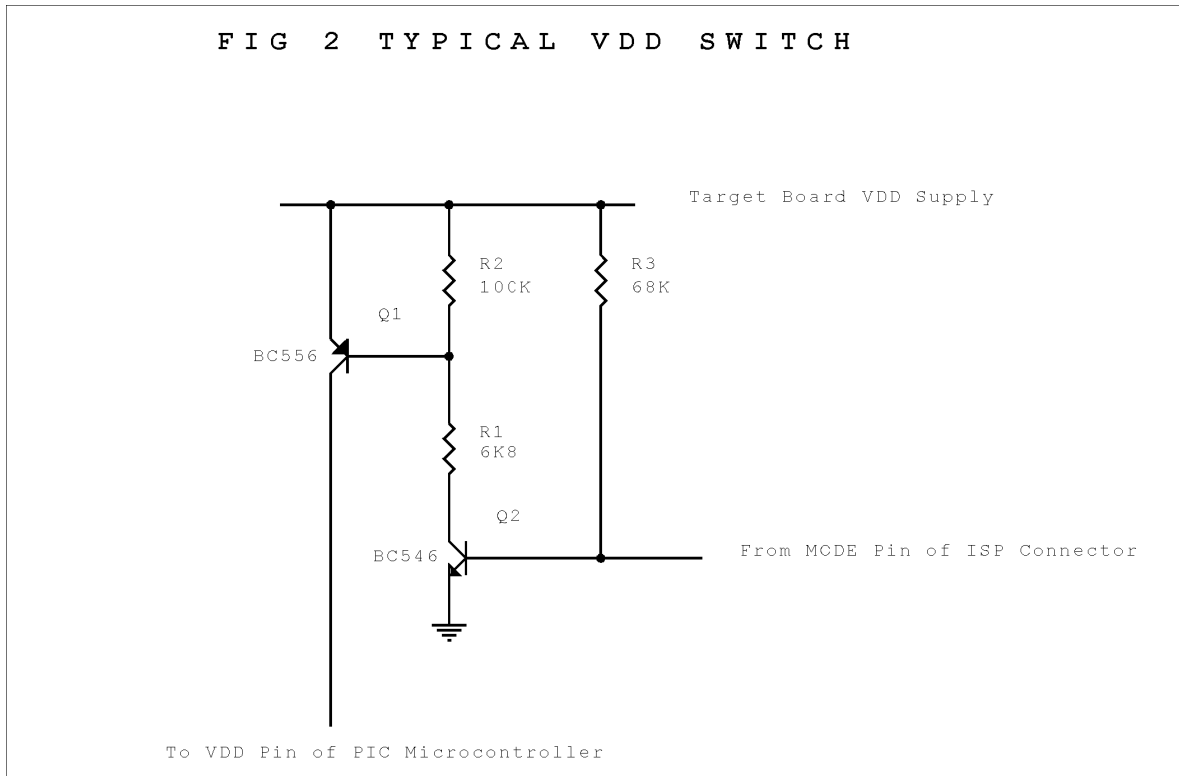
- **VDD**

The programming specification requires that during verification the supply voltage is varied over the full operating range of the device. The programmer could set the VDD supply anywhere between 2.7V and 6.0V depending on the device type. Verifying the device at the voltage limits ensures that the correct erase and programming margins have been achieved.

The VDD pin of the ISP connector must be directly connected to the VDD pin of the PIC. The design of the target board must be such that the programmer

can control the supply to the PIC without being

the reset circuit. A 1K resistor is required between

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           F I G   2   T Y P I C A L   V D D   S W I T C H



                                              Target Board VDD Supply

                          R2         R3
                          100K       68K

                 Q1

            BC556


                          R1
                          6K8

                          Q2
                                              From MODE Pin of ISP Connector
            BC546




           To VDD Pin of PIC Microcontroller
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affected by any other circuits on the board.

The maximum current that should be drawn from the programmer is 150mA at +5V. The maximum capacitance allowed on the VDD line is 10µF.

The target board may be completely powered from the programmer if its total requirements do not exceed those specified above.

In the event that the programmer VDD cannot be used to power the target board then the supply to the PIC must be isolated from that of the target board during programming. Isolation could be achieved with a simple removable link or automatically with a transistor switch. A typical example of a transistor switch is shown in fig 2.

- *VPP*

Pin 9 of the ISP connector must be connected to the MCLR/VPP pin of the PIC.

During programming the programmer applies a high voltage, typically 13.0V, to the VPP pin.

The programming specification requires a fast rise time for the VPP signal. There must be no capacitors directly connected to the VPP pin. Also VPP must not be allowed to pull VDD high, through

the VPP pin and the reset circuit.

OSCILLATOR

During the programming mode the normal oscillator circuit connected to the OSC1 and OSC2 pins of the PIC must be disabled. One way of achieving this is to apply ground or VDD to the OSC1 input. The signal could be derived from the MODE signal on the ISP connector.

PIC I/O PINS

Please note that during programming I/O pins are in the reset (high impedance) state.

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DEVICE PIN-OUTS

TABLE 1 - Device Pin-outs

Device Type: PIC16C61, 16C71

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
PDIP	14	4	12	13
SOIC	14	4	12	13
CERDIP	14	4	12	13

Device Type: PIC16C62, 16C62A, 16C72

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
SDIP	20	1	27	28
SOIC	20	1	27	28
SSOP	20	1	27	28
CERDIP	20	1	27	28

Device Type: PIC16C63, 16C66, 16C73, 16C73A, 16C76

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
SDIP	20	1	27	28
SOIC	20	1	27	28
CERDIP	20	1	27	28

Device Type: PIC16C64, 16C64A, 16C65, 16C65A, 16C67, 16C74, 16C74A, 16C77

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
PDIP	32	1	39	40
CERDIP	32	1	39	40
PLCC	35	2	43	44
MQFP	28	18	16	17

Device Type: PIC16C8X

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
PDIP	14	4	12	13
SOIC	14	4	12	13

Device Type: PIC16C554, 16C556, 16C558, 16C70, 16C71A, 16C710, 16C711, 16C620, 16C621, 16C622

PACKAGE	VDD	VPP	CLK(RB6)	DATA(RB7)
PDIP	14	4	12	13
SOIC	14	4	12	13
CERDIP	14	4	12	13
SSOP	16	4	13	14

Device Type: PIC12C508, 12C509, 12C508A, 12C509A, 12CE518, 12CE519

PACKAGE	VDD	VPP	CLK(GP1)	DATA(GP0)
PDIP	1	4	6	7
SOIC	1	4	6	7
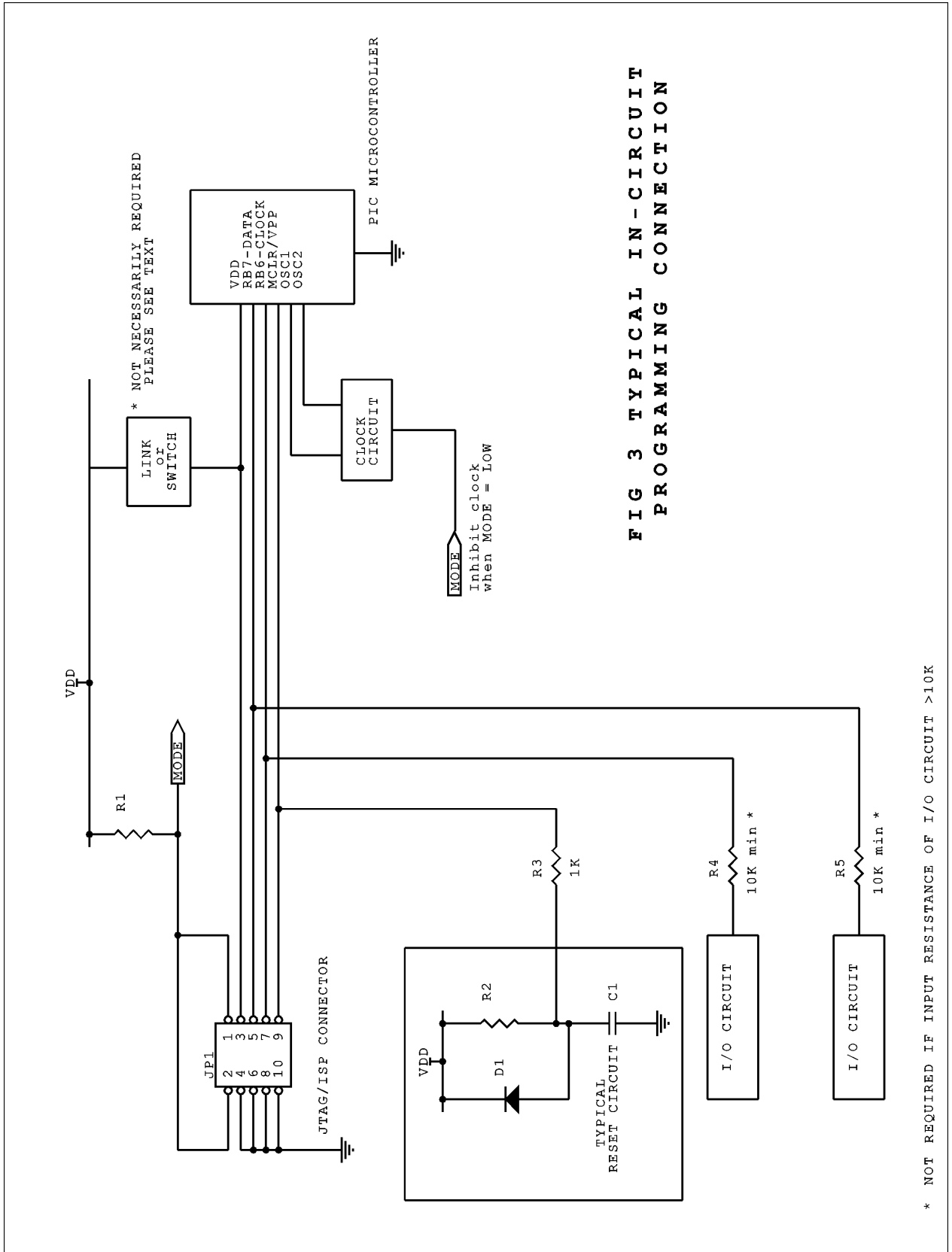
FIG 3 TYPICAL IN-CIRCUIT PROGRAMMING CONNECTION

ELECTRONICS

PROGRAMMING PROCEDURE

To avoid earth potential differences, if the target board is powered separately, the programmer and target board should be connected to a common mains supply.

- Connect the cable to the target board and the programmer.

- Power up the target board, if necessary, and proceed with programming in the normal way.

- If there are any other devices to be programmed on the board move the cable and repeat the procedure. This could be simplified by using a batch file which would automatically change the device type and instruct the operator where to plug in the cable.

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